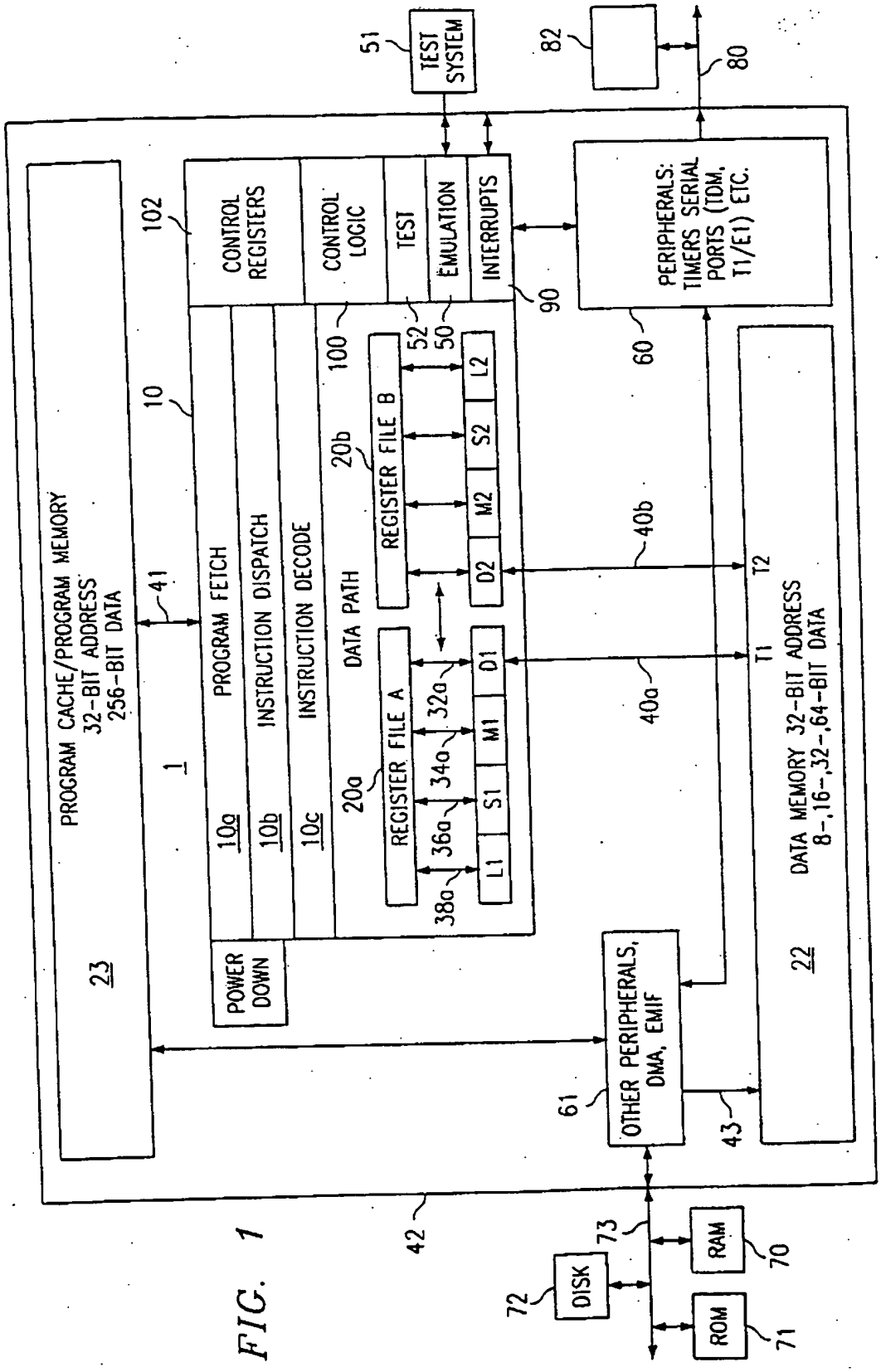
PROGRAM CACHE/PROGRAM MEMORY
32-BIT ADDRESS
256-BIT DATA
23
1
10
41
PROGRAM FETCH
INSTRUCTION DISPATCH
INSTRUCTION DECODE
DATA PATH
10a
10b
10c
20a
REGISTER FILE A
20b
REGISTER FILE B
CONTROL REGISTERS
102
CONTROL LOGIC
100
TEST
52
EMULATION
50
INTERRUPTS
90
L1
S1
M1
D1
L2
S2
M2
D2
36a
34a
32a
38a
POWER DOWN
TEST SYSTEM
51
82
80
PERIPHERALS: TIMERS SERIAL PORTS (TDM, T1/E1) ETC.
60
40b
40a
T2
T1
DATA MEMORY 32-BIT ADDRESS
8-,16-,32-,64-BIT DATA
22
OTHER PERIPHERALS, DMA, EMIF
61
43
42
73
DISK
72
RAM
70
ROM
71

FIG. 1

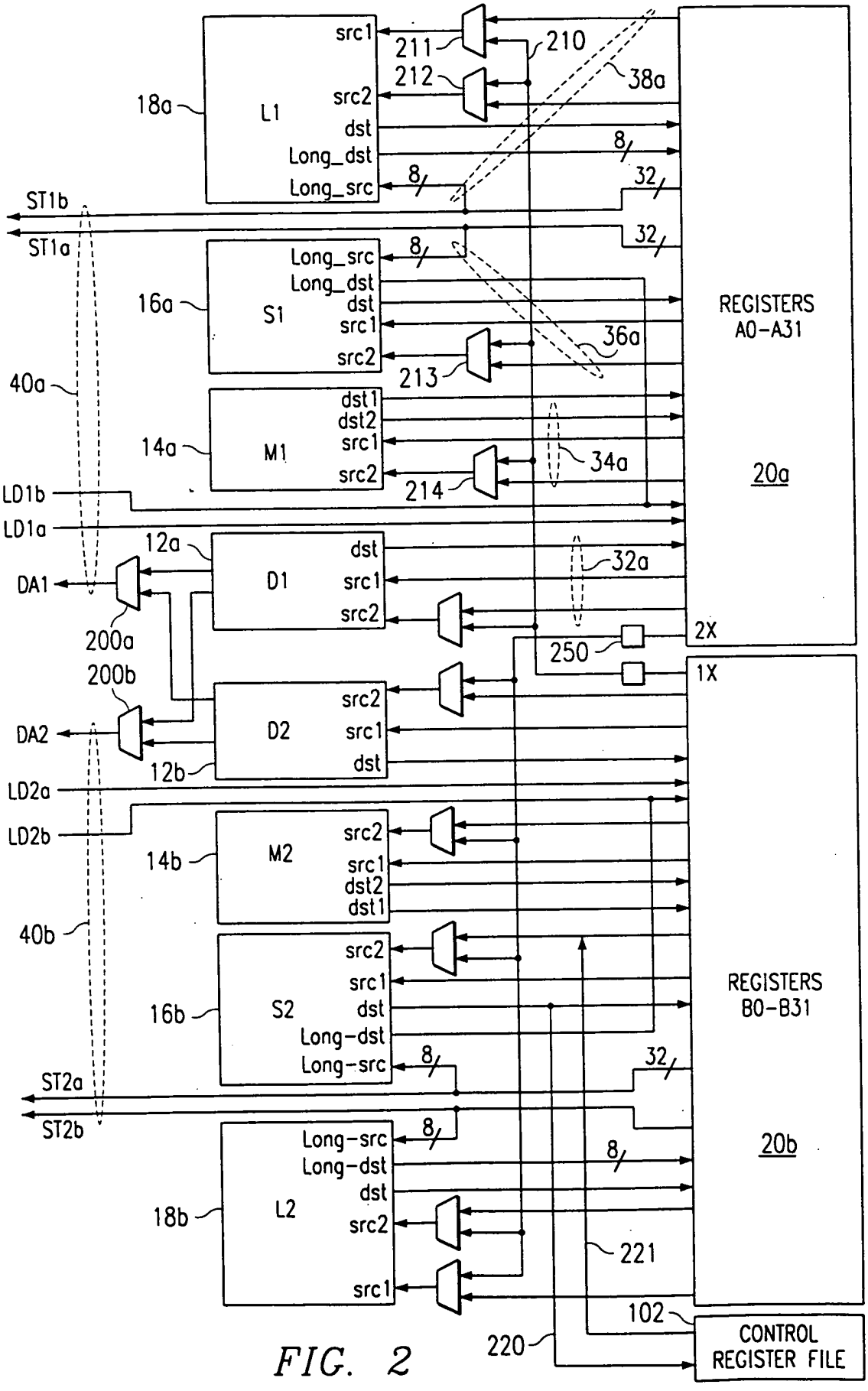

FIG. 2

DO NOT PHOTOCOPY

0075075 "0475075"

OPERATIONS ON THE .L UNIT

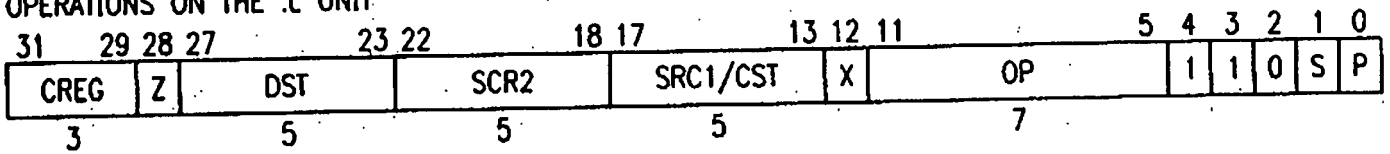

FIG. 3A

OPERATIONS ON THE .M UNIT

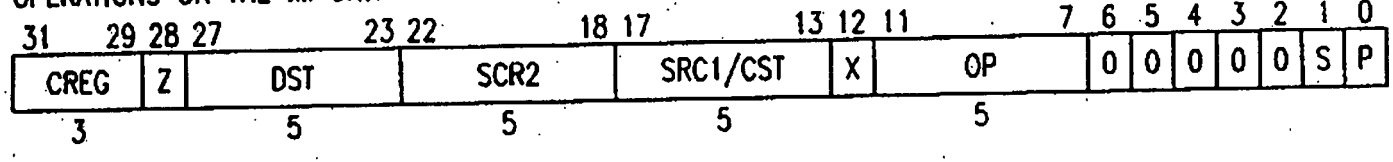

FIG. 3B

OPERATIONS ON THE .D UNIT

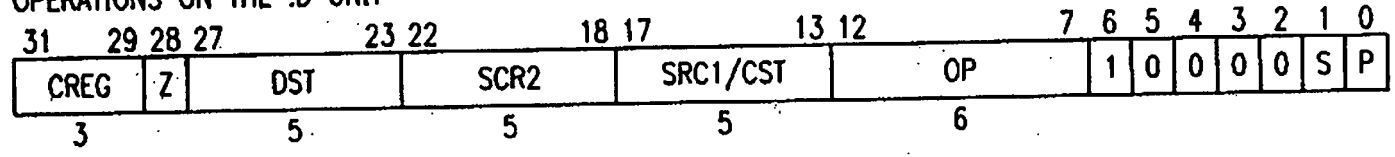

FIG. 3C

LOAD/STORE WITH 15-BIT OFFSET (ON THE .D UNIT)

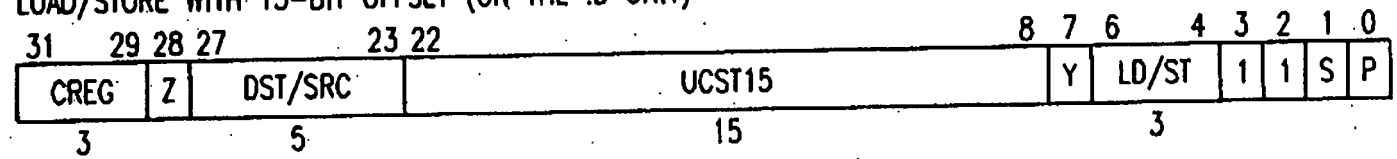

FIG. 3D

LOAD/STORE 'BASER' + 'OFFSETR/CST' ON THE .D UNIT

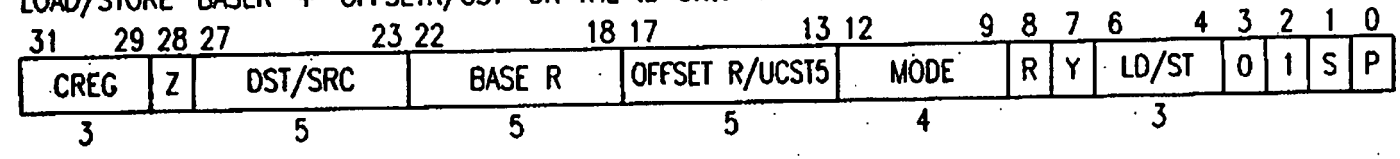

FIG. 3E

DOTSOT" 04TS0260

OPERATIONS ON THE .S UNIT

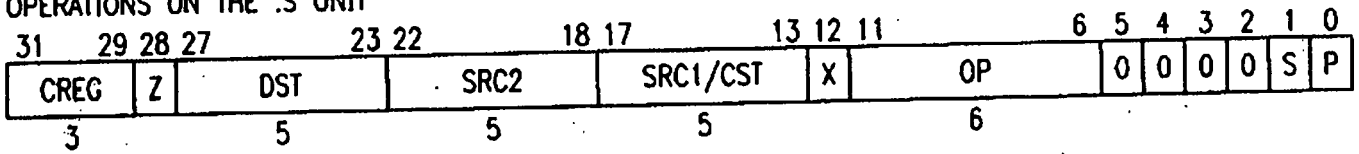

FIG. 3F

ADDK ON THE .S UNIT

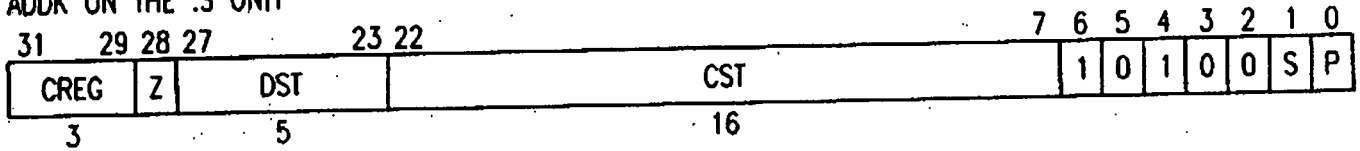

FIG. 3G

BITFIELD OPERATIONS (IMMEDIATE FORMS) ON THE .S UNIT

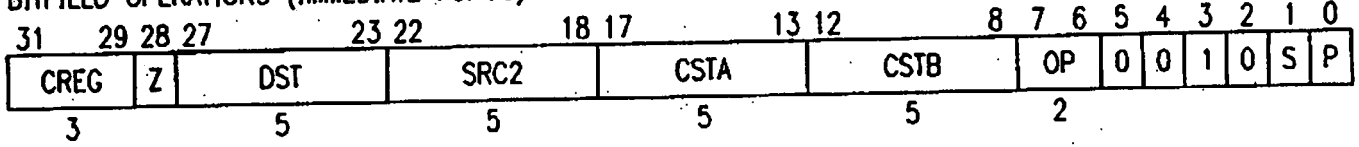

FIG. 3H

MVK AND MVKH ON THE .S UNIT

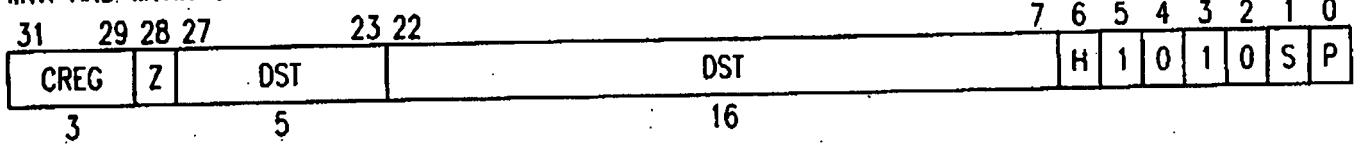

FIG. 3I

BCOND DISP ON THE .S UNIT

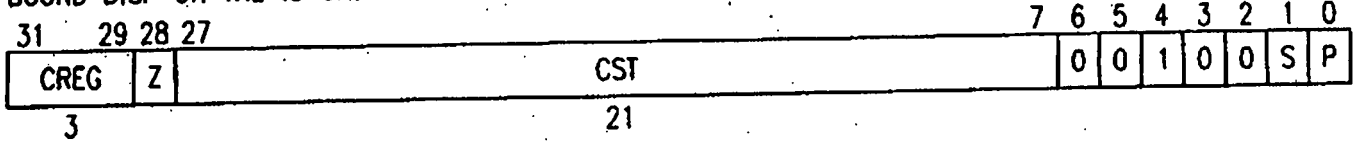

FIG. 3J

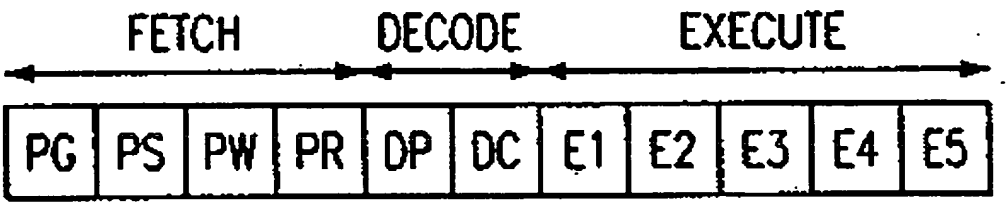

FIG. 4

DOTSOT" 04:T50460

OPERATIONS ON THE .M UNIT

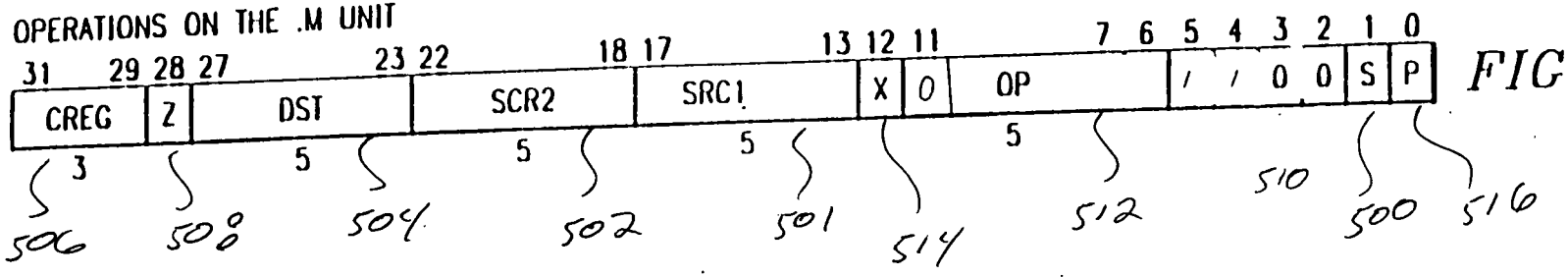

FIG. 5

6/12

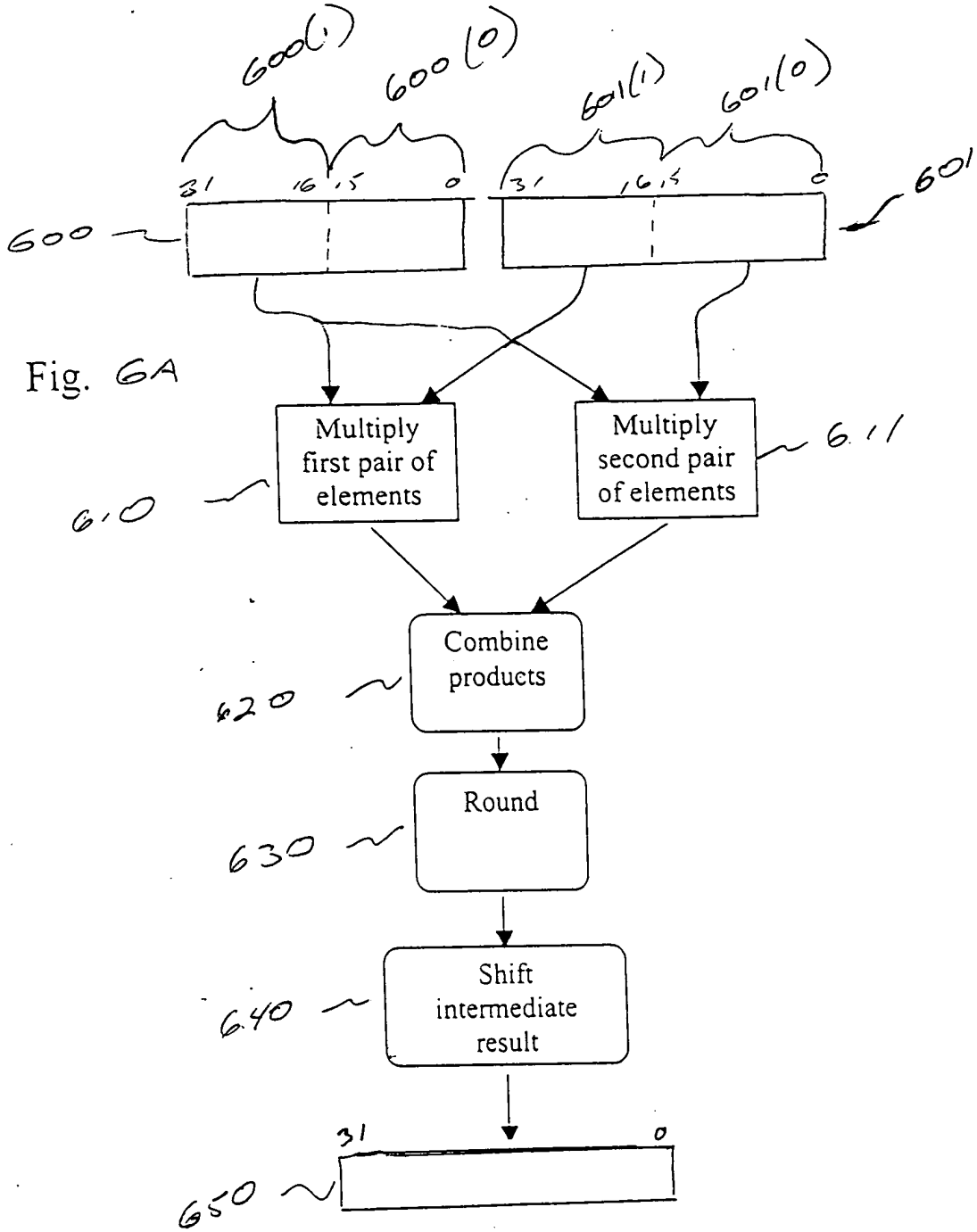
600(1)
600(0)
601(1)
601(0)
31
16
15
0
600
601
Multiply first pair of elements
Multiply second pair of elements
610
611
Combine products
620
Round
630
Shift intermediate result
640
650

Fig. 6A

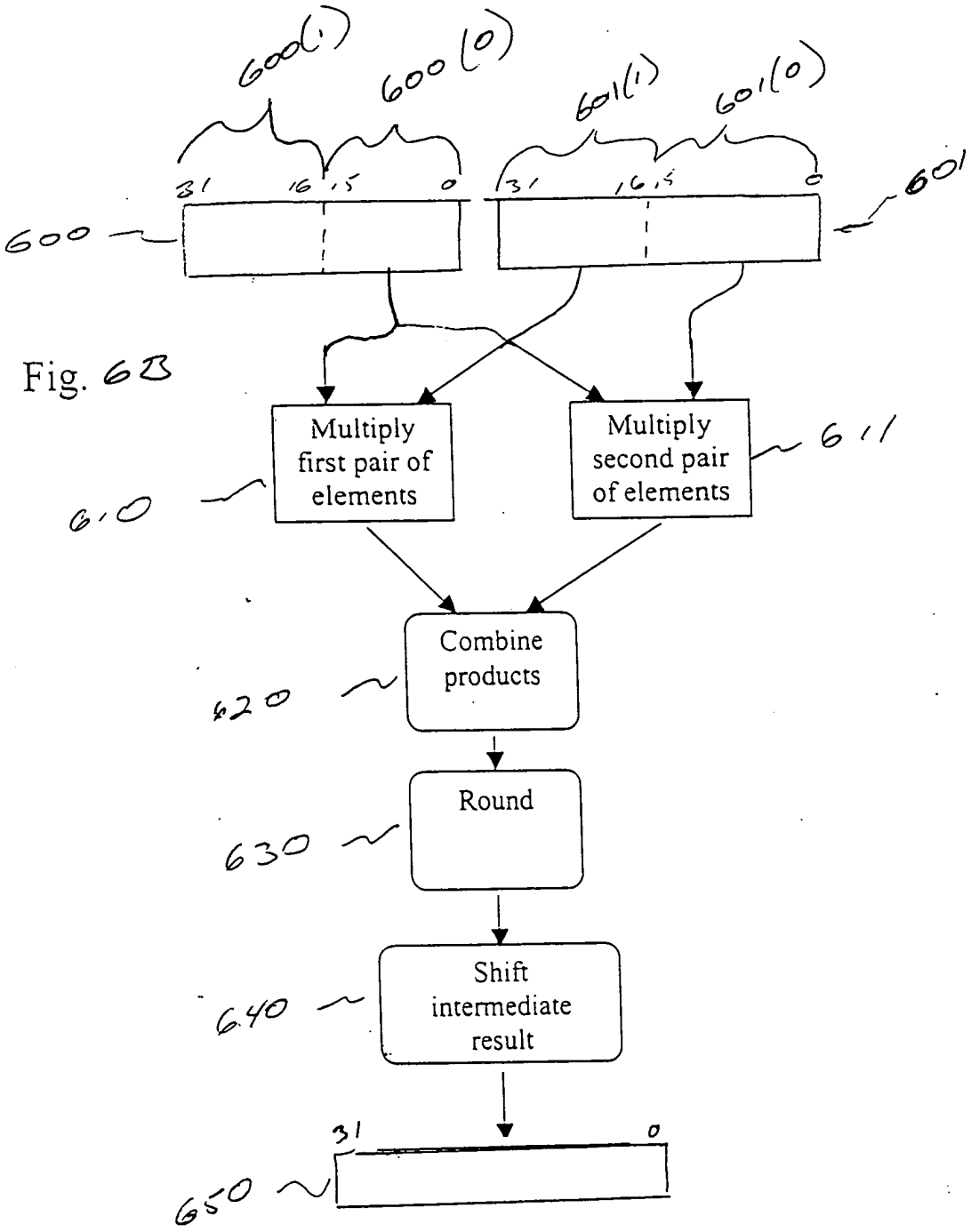
600(1)
600(0)
601(1)
601(0)
31
16
15
0
600
601
Multiply first pair of elements
Multiply second pair of elements
610
611
Combine products
620
Round
630
Shift intermediate result
640
650

Fig. 6B

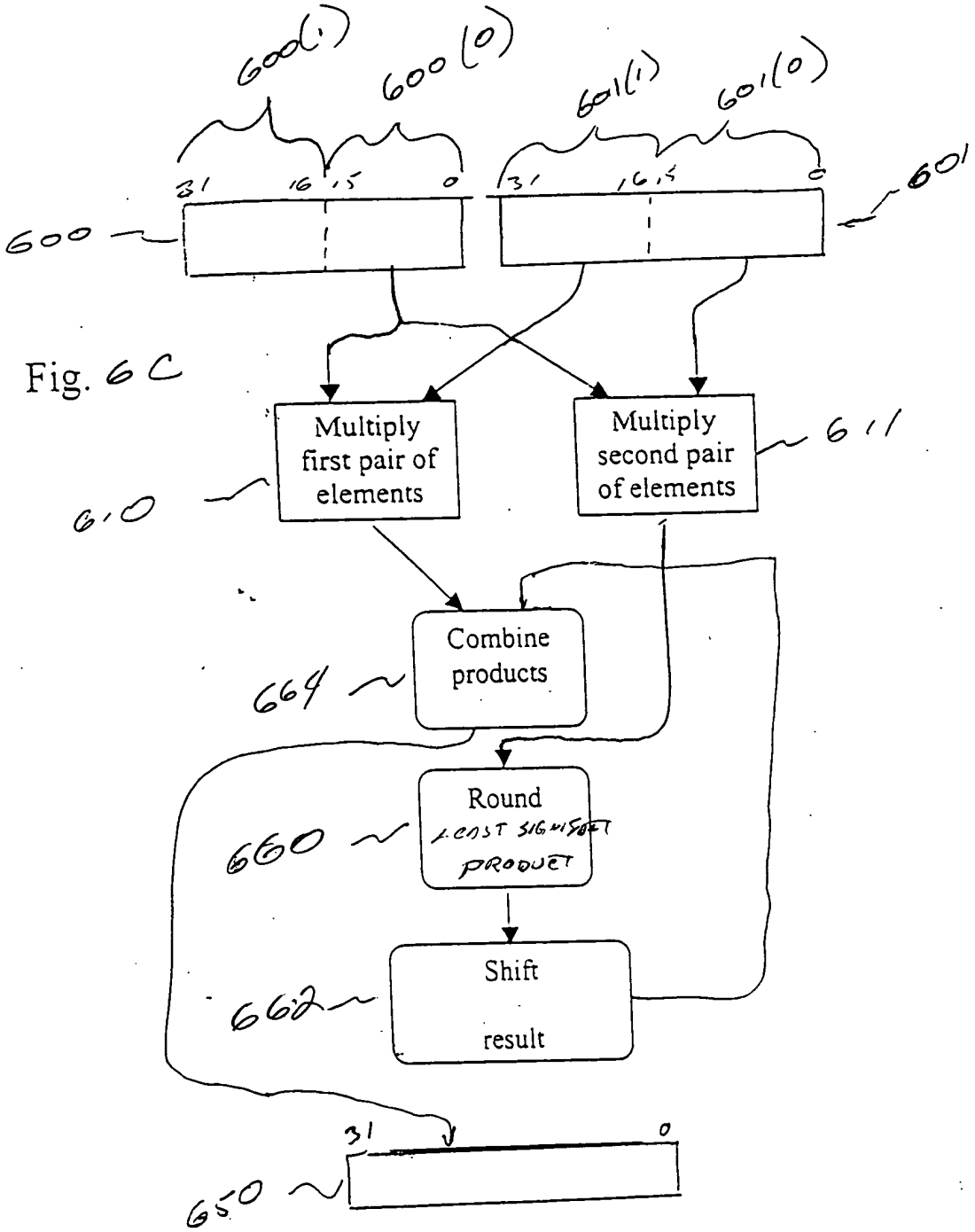
600(1)
600(0)
601(1)
601(0)
31
16
15
0
600
601
Multiply first pair of elements
Multiply second pair of elements
610
611
Combine products
664
Round
660
Shift
result
662
650

Fig. 6C

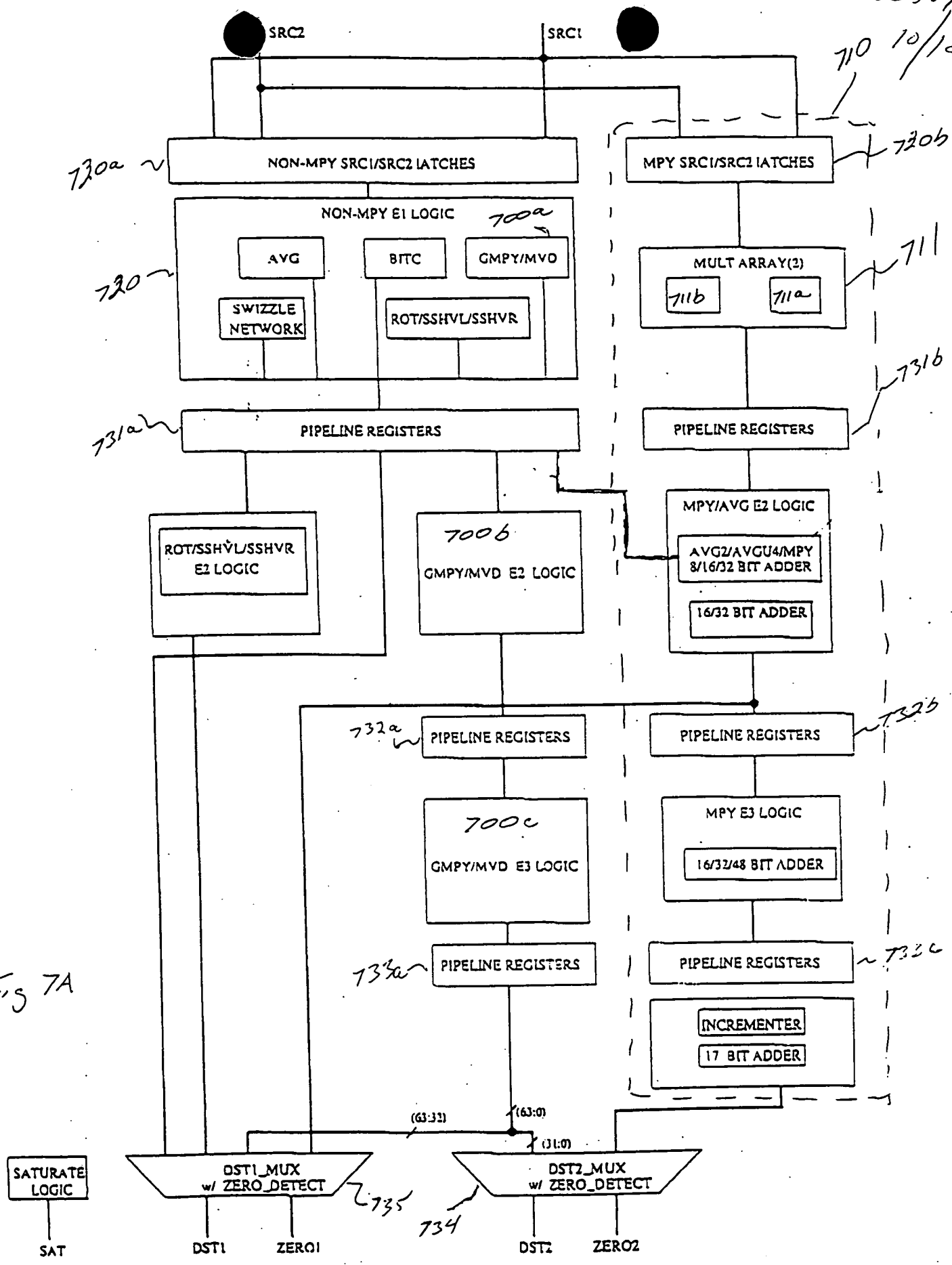
SRC2
SRC1
710
720a
NON-MPY SRC1/SRC2 LATCHES
720b
MPY SRC1/SRC2 LATCHES
NON-MPY E1 LOGIC
700a
AVG
BITC
GMPY/MVD
720
SWIZZLE NETWORK
ROT/SSHVL/SSHVR
MULT ARRAY(2)
711
711b
711a
731b
731a
PIPELINE REGISTERS
PIPELINE REGISTERS
ROT/SSHVL/SSHVR E2 LOGIC
700b
GMPY/MVD E2 LOGIC
MPY/AVG E2 LOGIC
AVG2/AVGU4/MPY 8/16/32 BIT ADDER
16/32 BIT ADDER
732a
PIPELINE REGISTERS
PIPELINE REGISTERS
732b
700c
GMPY/MVD E3 LOGIC
MPY E3 LOGIC
16/32/48 BIT ADDER
733a
PIPELINE REGISTERS
PIPELINE REGISTERS
733b
INCREMENTER
17 BIT ADDER
(63:32)
(63:0)
(31:0)
SATURATE LOGIC
DST1_MUX w/ ZERO_DETECT
735
DST2_MUX w/ ZERO_DETECT
734
SAT
DST1
ZERO1
DST2
ZERO2

Fig 7A

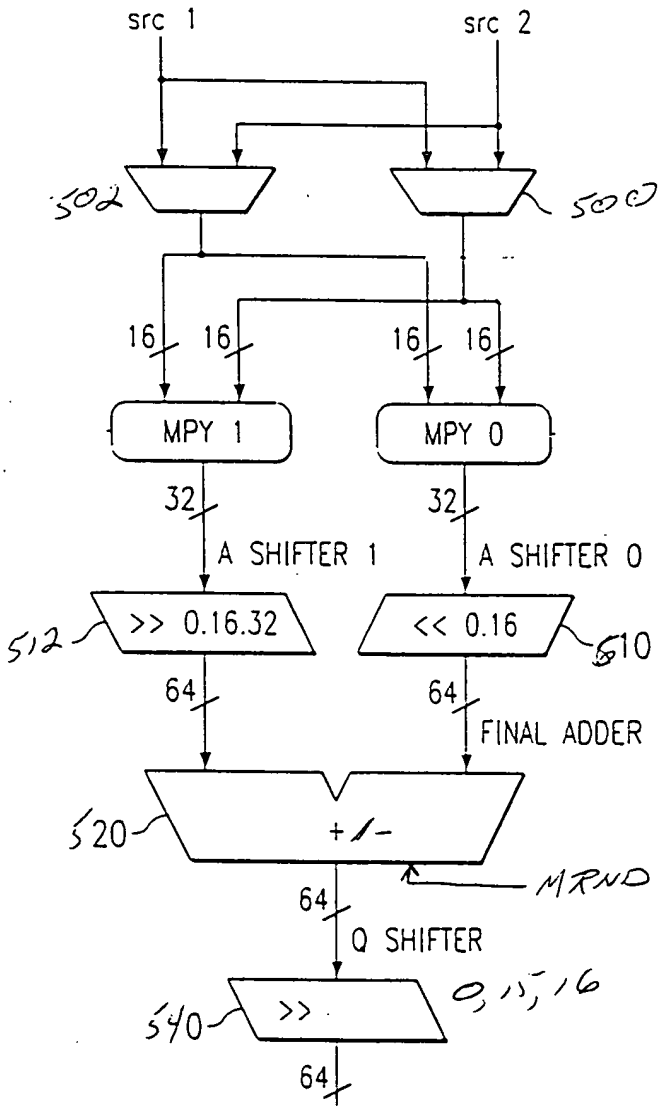

FIG. 7B

CUTTER CYL

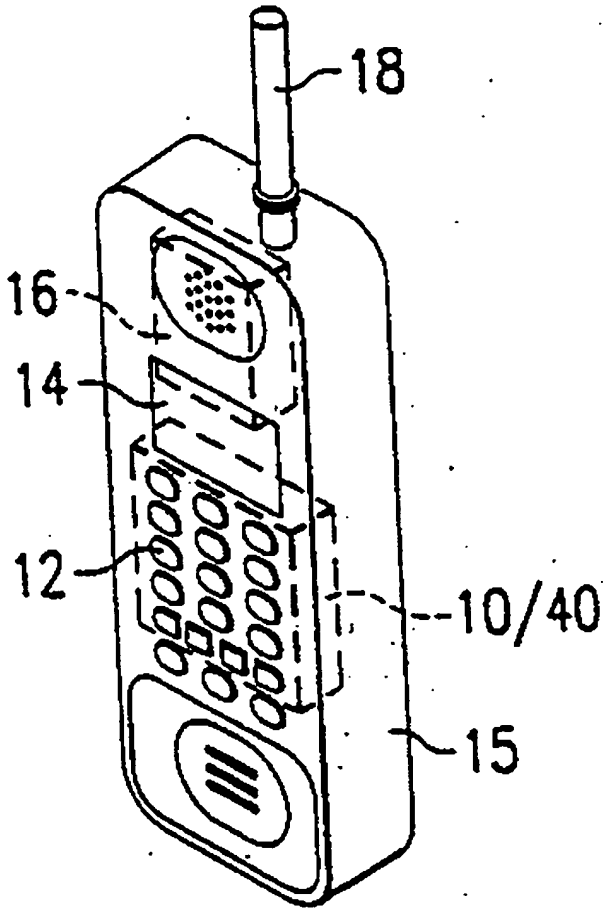

Fig 8

DATE SENT: 04/25/2000